12 GHz Low-Noise MMIC Amplifier Designed with a Noise Model that Scales with MODFET Size and Bias

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***Abstract*—A scalable, bias-dependent FET noise model was developed for MMIC design. A three-stage, 12 GHz, MMIC, low-noise amplifier (LNA) was designed with the model. The LNA has a 1.6 dB noise figure and 25.6 dB gain. Lumped elements were used to design an LNA that was significantly smaller per stage (0.31 mm^2) than previous MMIC LNA's.**

I. Introduction

MMIC's are gradually replacing hybrid MIC's in commercial applications. Downconverters for 12 GHz direct broadcast satellite (DBS) receivers have found wide acceptance [1]. However, the LNA of most 12 GHz DBS rceivers is still a hybrid MIC. Successful replacement of hybrid MIC's with MMIC's requires similar or better performance and reliability with higher manufacturability and lower cost. This paper describes a design that addresses manufacturability and cost through small chip size.

Another market for MMIC's is custom IC's. Time to market and the cost of engineering design are important for these markets. Success on the first design iteration is key. This requires accurate computer-aided design models. This paper describes a noise model that was developed for MMIC design. The noise model scales with FET size and FET bias. The model was used successfully to design the 12 GHz LNA.

II. MMIC Technology

This MMIC process was developed for high-performance instrument applications, such as broadband power amplifiers [2], [3]. However, the process is useful for a variety of applications [4]. The active devices are modified 25% In pseudomorphic MODFET's, with *e*-beam written, 0.25 μm, Ti/Pt/Au mushroom gates [5]. The PMODFET's typically have a maximum f_T greater than 70 GHz, $I_{D\max}$ of 520 mA/mm, and V_{Bgdo} of -11 V (1 mA/mm). The process has respectable power and noise performance: maximum output power is 700 mW/mm at 40 GHz and $F_{\min}$ is 0.8 dB with G_a of 13 dB at 12 GHz. The process uses tantalum nitride thin-film resistors (22 $\Omega/\square$), bulk resistors, (220 $\Omega/\square$), silicon nitride MIM capacitors (0.60 pF/μm^2), two levels of interconnect metal, and 40 $\times$ 40 μm backside vias (27 pH) [4]. Critical parameters are controlled to better than 16%. The PMODFET's are reliable with an MTTF greater than 10^6 h at a channel temperature of 150°C. The process was used to fabricate 2–50 GHz TWA's with 9 dB gain and 20 dBm output power [6].

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III. FET Noise Model

The bias-dependent FET noise model was developed from the noise temperature model of Pospieszalski [7], [21]. The noise model of the intrinsic FET is shown in Fig. 1. The model uses only uncorrelated thermal noise from the resistors. The input resistor r_{gs} is at ambient temperature T_g. The output resistor R_{ds} is at temperature T_d. T_d is typically 2000 K for a FET biased for lowest $F_{\min}$. T_d is extracted directly from measured noise data and the FET circuit model. The noise model for the extrinsic FET includes thermal noise from the parasitic resistors R_s, R_g, and R_d at ambient temperature. The model was implemented into a bias-dependent FET model in the HP Microwave Design System [11]. The noise model is not applicable where noise from gate leakage current and $1/f$ noise are significant. These additional noise sources were negligible for the PMODFET's measured at low noise biases. After careful deembedding of parasitics, the correlation between input and output noise was approximately zero ($|C| < 0.1$).

This model accurately predicts all four noise parameters as function of frequency using a single modeling parameter: the noise temperature of the output resistor T_d [7]–[9]. Excellent agreement between measured and modeled $F_{\min}$ and G_a are shown in Fig. 2. The agreement between measured and modeled S_{11}, S_{22}, and Γ_{opt} (generator reflection coefficient for minimum noise figure) is demonstrated in Fig. 3.

A noise model that scales with width is essential for MMIC design because FET's of different widths are used and the width is optimized in circuit design. The noise model scales with FET size because T_d is a very weak function of width. The circuit model elements have standard scaling: the capacitances and transconductance are proportional to width, and the intrinsic and extrinsic re-

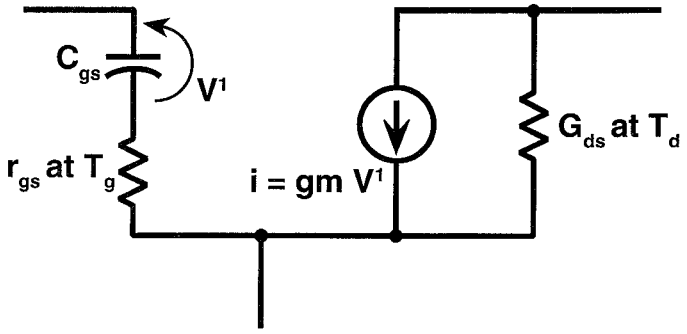

Fig. 1. Noise model for an intrinsic FET.

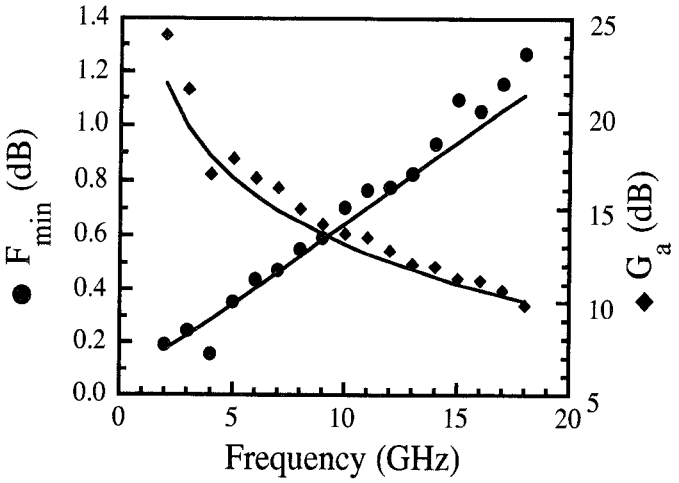

Fig. 2. Plot of measured and modeled F_{min} and G_a versus frequency for a 180 μm wide PMODFET biased at I_{ds} of 60 mA/mm and V_{ds} of 2 V.

sistors are inversely proportional to width. An example of circuit and noise model scaling is shown in Fig. 4 for PMODFET's with interdigitated fingers. The number of fingers is varied by adding fingers in parallel. The normalized extrinsic input resistance R_{in} · width and the normalized optimum generator resistance R_{opt} · width are weak functions of the number of fingers for PMODFET's with fingers 30 and 45 μm wide. Increasing the finger width increases R_{in} · width and R_{opt} · width, as expected, because the normalized gate resistance R_g · width increases in proportion to the finger width squared.

Simulation of MMIC noise figure is needed not only for low-noise amplifiers, but for MMIC's with other design goals (e.g., broad-band gain, or low dc power consumption, etc.). Therefore, a bias-dependent noise model is useful for MMIC design. A bias-dependent noise model was developed by making T_d a function of I_{ds} and V_{ds} [8], [10]. The T_d function is empirical and made to fit the data best where F_{min} is lowest. The bias-dependent linear FET circuit model is similar to the HP Root nonlinear FET model in that it is directly constructed from automatically characterized device data [11]. The circuit model scales well so that the noise data for the 180 μm wide PMODFET were fit to a scaled circuit model of a 240 μm wide

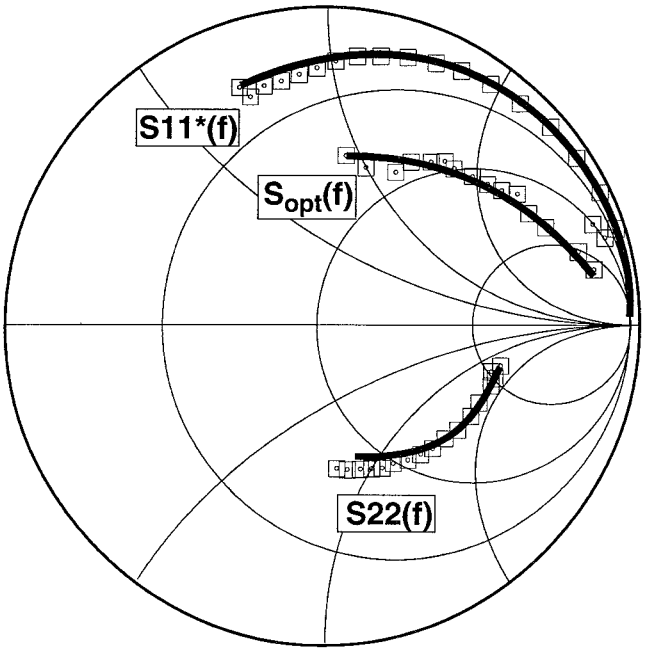

Fig. 3. Smith chart plot of measured and modeled Γ_{opt}, S_{22}, and S_{11}^* versus frequency (2–18 GHz) for a 180 μm wide PMODFET biased at I_{ds} of 60 mA/mm and V_{ds} of 2 V.

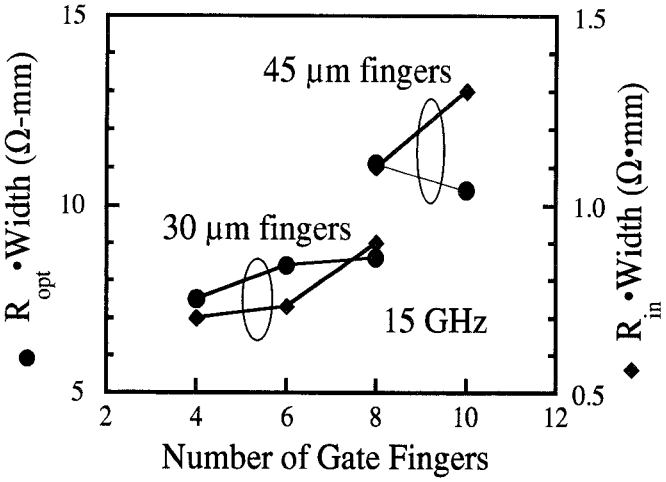

Fig. 4. Plot of measured normalized optimum source resistance at 15 GHz R_{opt} · width and extrinsic input resistance R_{in} · width versus number of fingers for a 0.25 μm PMODFET with V_{ds} of 2 V and I_{ds} of 60 mA/mm.

PMODFET. Comparisons of the measured and modeled F_{min} and G_a at 12 GHz versus I_{ds}/width and V_{ds} are shown in Figs. 5 and 6. The PMODFET's have a broad bias range where F_{min} is low, as shown in Figs. 5 and 6. The low-sensitivity F_{min} to bias makes LNA's more manufacturable with PMODFET's. The usefulness of the bias-dependent scalable noise model was demonstrated with the simulation of a 0.5–50 GHz distributed amplifier that employs cascoded MODFET's [3]. There was good agreement between measured and simulated noise figures up to 50 GHz [3].

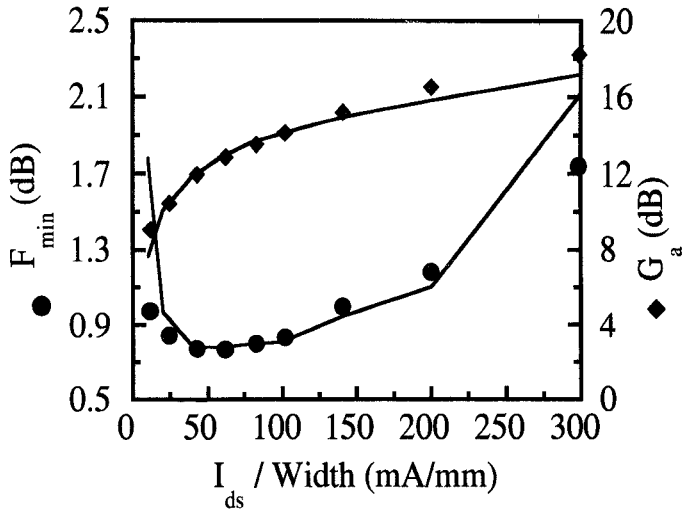

Fig. 5. Plot of measured and modeled F_{min} and G_a at 12 GHz versus I_{ds}/width for a 180 μm wide PMODFET with V_{ds} of 2 V.

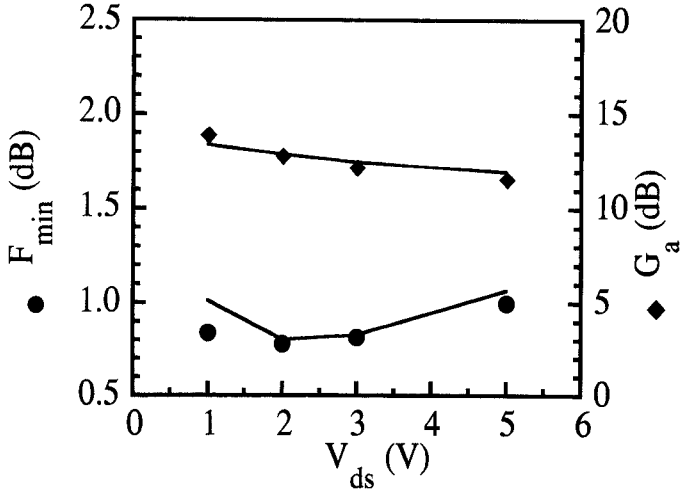

Fig. 6. Plot of measured and modeled F_{min} and G_a at 12 GHz versus V_{ds} for a 180 μm wide PMODFET with I_{ds}/width of 60 mA/mm.

IV. Amplifier Design

The noise model was used to design a three-stage 12 GHz low-noise MMIC amplifier with the HP Microwave Design System MDS. The design goals were lowest noise figure, more than 25 dB gain, small chip size, and input and output return loss greater than 10 dB. For a FET with low F_{min} (<1.0 dB) and high G_a (>10 dB), the optimum generator impedance differs significantly from the generator impedance for maximum gain. When a FET is matched for maximum gain, the amplifier input return loss is very high. Therefore, when an amplifier is designed for F_{min}, then the input return loss cannot be high. Like many other circuit design problems, performance can be impoved at the cost of gain. Source inductance (negative feedback) was added to the PMODFET to improve the amplifier input return loss with little effect on F_{min}, but at the cost of gain. Source inductance was synthesized with a high-impedance (9 μm wide) microstrip line. The tradeoff between gain and return loss was simulated in the HP-MDS by sweeping the length of the source line, as shown in Fig. 7. Return loss improves 2.9 dB/1 dB loss of gain. A transmission line length of 200 μm was chosen as a compromise for the 360 μm wide FET.

FET width is a useful design parameter for MMIC designers. The scalable device model was used to select a FET width for broad noise circles [12] and a simple input matching network (shunt inductance). Noise circles are broader for a FET with a smaller $|\Gamma_{opt}|$ (i.e., angle of Γ_{opt} near 90°). Source inductance also makes the noise circles broader because the noise parameter n ($4NT_o/T_{min}$) is larger [12]. The FET width was chosen so that Γ_{opt} lies on the 1/50 Ω admittance circle. Then, the input matching network was a simple shunt inductor. A simple matching network is preferred because it should be smaller and more likely correct. Fewer, smaller passive matching components are preferred because MMIC passive components are not high Q and degrade the noise figure of the LNA.

The number of gate fingers was chosen for the minimum noise figure for a given total width. Shorter fingers result in a lower R_g (end-to-end R_g was 250 Ω/mm). However, more fingers are needed for the same total width and the parasitic gate–source crossover capacitance increases (4 fF/crossover). 12 fingers was the best compromise for the 360 μm FET in this PMODFET process.

Small chip size and single-supply non-tweaked bias are essential for MMIC's in cost-competitive commercial markets such as DBS. Lumped components are necessary for small chips. The matching networks were designed with MIM capacitors and spiral inductors. The biasing and matching networks were combined for size and simplicity, as shown in Fig. 8. The three-stage amplifier was made by cascading three identical stages. A photograph of the finished circuit is shown in Fig. 9.

The I_{ds} for lowest F_{min} is small (60 mA/mm); therefore, it is very sensitive to V_p changes due to process variations (e.g. doping density and gate recess depth). I_{ds} must change less than ±25 mA/mm to assure that F_{min} increases less than 0.1 dB. The following sensitivity analysis shows that I_{ds} at a fixed V_{gs} cannot be controlled adequately with our PMODFET process. Near pinch off, I_{ds} has approximately square law behavior:

$$I_{ds} = \beta(V_{gs} - V_p)^2 = \frac{g_m}{2}(V_{gs} - V_p) \tag{1}$$

where β is a fitting factor. The sensitivity of I_{ds} to the pinch off voltage is $-g_m$:

$$\frac{\partial I_{ds}}{\partial V_p} = -2\beta(V_{gs} - V_p) = -g_m. \tag{2}$$

At the I_{ds} for lowest F_{min}, the PMODFET has a g_m of 290 mA/mm. Therefore, V_p should be controlled to ±86 mV, which is less than the process control limit for V_p of 300 mV.

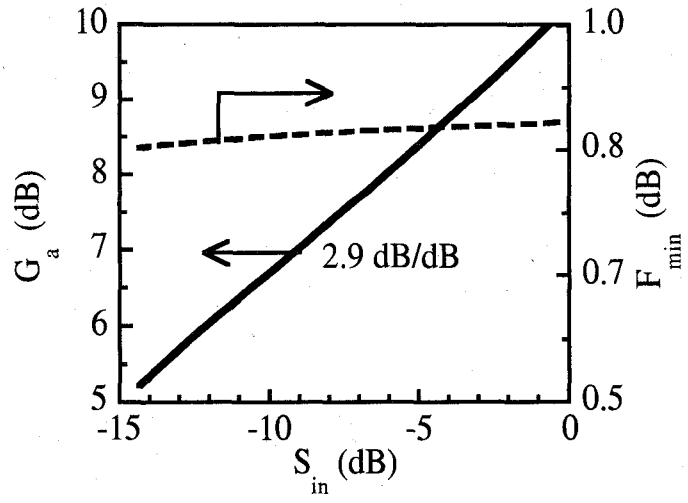

Fig. 7. Plot of G_a and $F_{\min}$ versus S_{11} for a 12 GHz ideal LNA. Parameters were changed by sweeping the length of a high-impedance source line.

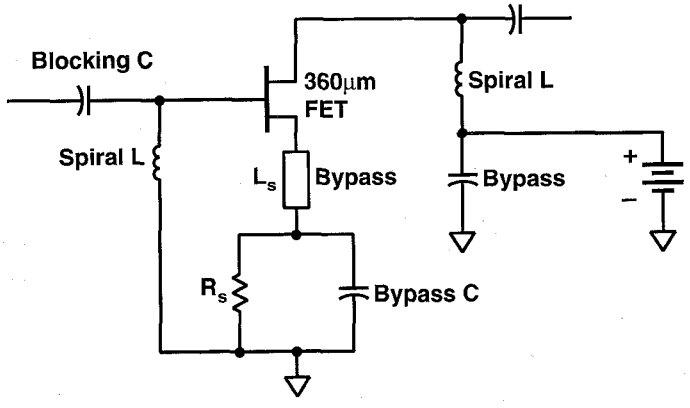

Fig. 8. Circuit schematic for a single stage of the 12 GHz LNA.

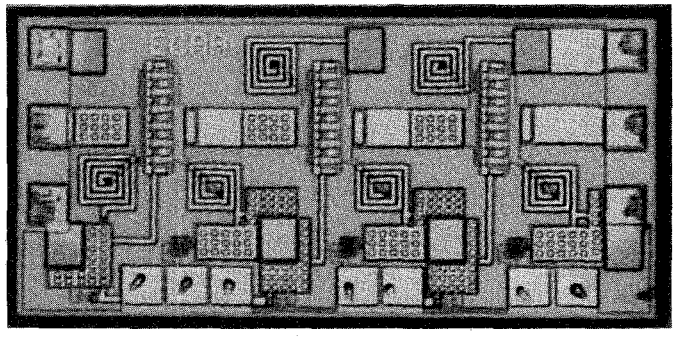

Fig. 9. Photograph of the three-stage 12GHz MMIC LNA.

Source resistance bypassed with a capacitor was incorporated in the design to reduce the sensitivity to V_p and thus enhance manufacturability of the LNA. It is well known that R_s reduces the extrinsic g_m of a FET by $1/(1 + g_m \cdot R_s)$. The sensitivity of I_{ds} to V_p is reduced by the same factor. For a PMODFET I_{ds}/width of 60 mA/mm, V_{gs} was -0.78 V. The LNA was designed to operate with the gate at dc ground and a single bias supply at the drain by selecting R_s for $R_s \cdot I_{ds} = 0.78$. In this LNA design, the V_p sensitivity was reduced by a factor of 5. The LNA, with R_s, could tolerate a V_p variation of ± 430 mV before the noise figure increased 0.1 dB; therefore, it was manufacturable. Biasing was reproducible; the standard deviation for drain current was 5.2 mA/mm (8%) for three wafers. The effect of R_s is demonstrated with two wafers with a 0.2 V difference in V_p. The difference could have caused an 80% difference in I_{ds} at fixed V_{gs}. However, the I_{ds} of the LNA's with the source resistance biasing changed only 16%. A larger source resistance was not used because it would require the extra complexity of biasing the gate and dissipating more than 28% of the dc power in the source resistors. R_s degrades the RF gain and increases thermal noise. To minimize these problems, R_s was bypassed with a 6 pF capacitor, as shown in Fig. 8.

V. Measured Microwave Performance

The three-stage 12 GHz LNA's had a mean noise figure of 1.6 dB with a mean gain of 25.6 dB. The input and output return losses were 13 dB and greater than 25 dB, respectively. The frequency dependence of gain and noise figure is shown in Fig. 10. The noise figure was measured on-wafer with a noise figure meter. The 0.1 dB ripple on the noise figure versus frequency is attributed to the variation of on-wafer source match with frequency. The standard deviations for three wafers for gain and noise figure were 0.5 and 0.08 dB, respectively. The small standard deviations are attributed to the reproducible biasing and the process parameter control. The best performance was a noise figure of 1.53 dB with 25.5 dB gain. The electrical yield of the circuit was 91%. The input and output return losses are better than 10 dB across the band, as shown in Fig. 11. The isolation was better than 35 dB. The noise figure, gain-per-stage and return-loss are comparable or better than most 12 GHz MMIC LNA's, as shown in Table I. The MMIC was biased with a single supply of 2.75 V drawing 73 mA.

The noise figure and gain of the LNA are a weak function of the supply voltage, as shown in Fig. 12. The low sensitivity of the LNA to supply voltage should make the LNA simpler to use and modules more manufacturable.

VI. Discussion

The most remarkable feature is the MMIC size. The chip was only 0.92 mm^2 or 0.31 mm^2/stage. This chip size per stage is significantly smaller than previously reported 12 GHz MMIC LNA's. A comparison of 12 GHz MMIC LNA's is given in Table I. The LNA reported here is less than half the size per gain stage of the previous smallest LNA.

The noise figure modeled for the LNA was 1.3 dB. A difference of 0.3 dB is not significant for most gain simulations, but important for noise figure. The 0.3 dB difference could be attributed to: 1) coupling between components, 2) underestimate of passive component losses, 3) process variation, and 4) measurement errors. The in-

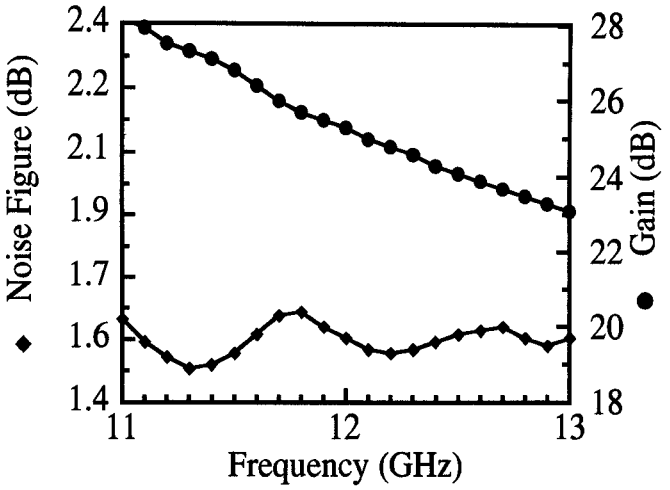

Fig. 10. Plot of measured noise figure and gain of LNA versus frequency.

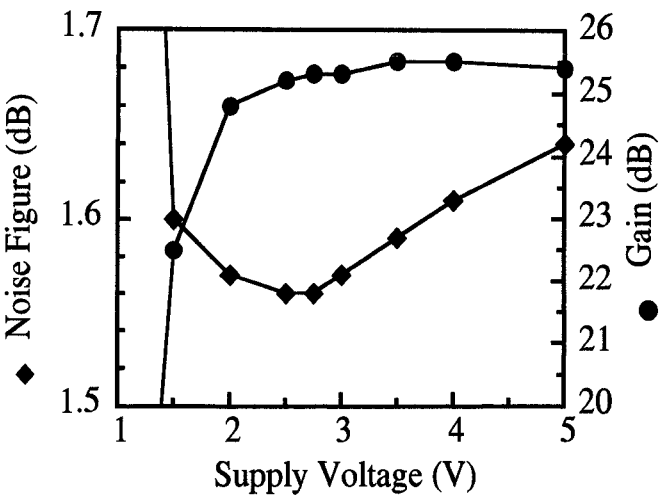

Fig. 12. Plot of measured noise figure and gain of LNA at 12 GHz versus supply voltage.

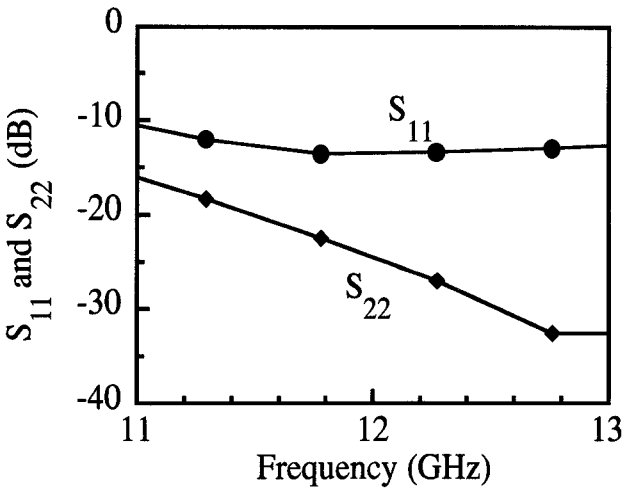

Fig. 11. Plot of measured input and output return losses of MMIC LNA versus frequency.

TABLE I
COMPARISON OF 12 GHZ MMIC LOW-NOISE AMPLIFIERS

Company	Ref.	Stages	F_{min} dB	F db	G/stage dB	Area/Stage mm^2/#
HP	—	3	0.86	1.6	8.2	0.31
Sharp	[20]	2	—	2.5	8.3	0.72
Sumitomo	[13]	4	0.7	1.1	6.5	1.20
Sumitomo	[14]	4	1.2	1.7	6.0	2.25
Hitachi	[15]	2	1.1	1.3	7.7	1.50
Matsushita	[16]	2	0.5	1.2	8.2	1.63
Mitsubishi	[17]	2	1.0	1.6	7.0	1.96
NEC	[18]	2	1.7	2.8	8.0	0.65
Toshiba	[19]	3	1.9	3.4	6.6	1.50

put return loss was better than modeled. This indicates that the input matching network was not optimum for the lowest noise figure. The compact layout of the circuit results in unmodeled coupling between components. Coupling was probably a major cause of performance less than modeled.

VII. CONCLUSIONS

A scalable, bias-dependent FET noise model was developed for MMIC design. The FET noise model is based on the resistor temperature noise model of Pospieszalski. The noise temperature of the output resistor was made a function of I_{ds} and V_{ds} in a measurement-based bias-dependent linear circuit model. All four noise parameters were modeled for PMODFET's of different widths, numbers of fingers, and biases.

A three-stage, 12 GHz, MMIC low-noise amplifier was designed with the noise model. The LNA has an average noise figure of 1.6 dB with 25.6 dB gain. An RF bypassed source resistor was employed for biasing with a single power supply and for improved tolerance of process variations. Source inductance was added to obtain both low noise figure and acceptable input match. The FET width was chosen for broad noise circles and a simple input matching network. The LNA chip was designed significantly smaller per stage (0.31 mm^2/number) than previous MMIC LNA's by using lumped elements such as spiral inductors.

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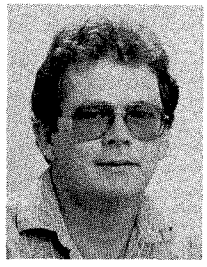
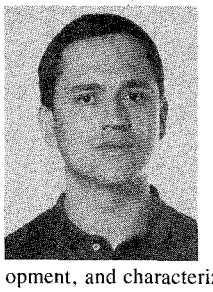


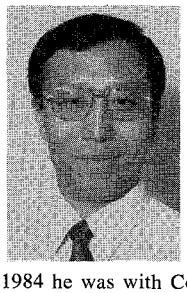
Brian Hughes (M'89) received the B.Sc. (Hons.) degree in material science from Queen Mary College, University of London, and the Ph.D. degree in material science from the University of Southern California, Los Angeles. His dissertation was entitled, "A transmission electron microscopy study of ion implanted GaAs."

He joined the Hewlett-Packard Microwave Technology Division, Santa Rosa, CA, in 1979, to investigate why undoped GaAs was semi-insulating. Next, he gained insights into the origins of flicker noise, and reduced the $1/f$ noise corner of GaAs MESFET's to 1 MHZ. He helped develop a theory and method for predicting phase noise in microwave oscillators. He was a Visiting Scientist at Cornell University with Prof. Eastman's group in 1988. He was an HP Faculty Loan Professor at the University of California, Santa Barbara, in 1990 where he taught a course entitled, "Design and characterization of high frequency devices." He has designed and characterized mm-wave pseudomorphic power MODFET's. His current interests are techniques for measuring power and noise figure of FET's and extracting their models. He is currently designing low-noise MODFET MMIC amplifiers.



Julio Perdomo received the B.Sc., M.S., and Ph.D. degrees from Cornell University in 1978, 1980, and 1983, respectively. His doctoral dissertation was on the modeling and characterization of the avalanche breakdown response time in Si tunnel diodes.

In 1983 he joined the Microwave Technology Division of Hewlett-Packard Company where he worked in the development of measurement systems to characterize FET's at mm waves. Since 1989 he has been involved in the design, development, and characterization of mm-wave IC's.



Hiroshi Kondoh (S'72–M'75) received the B.S. and M.S. degrees in electronics from Shizuoka University, Japan, in 1973 and 1975, respectively, and the Ph.D. degree in electrical engineering from Cornell University, Ithaca, NY, in 1982.

He was a full-time Research Fellow at the Research Institute of Electronics, Shizuoka University, from 1975 to 1983, where he worked on a microwave-biased photodetector and on wide-band IMPATT and GUNN oscillators. From 1983 to 1984 he was with Cornell University as a Visiting Scientist, involved in the development of a mm-wave vector network analyzer. He joined Hewlett-Packard, Microwave Technology Division, in 1984 as a member of the Technical Staff to work on MMIC circuit designs and FET characterization. Since 1988 he has been an R&D Project Manager at Hewlett-Packard. He has supervised the development of a 50 GHz MODFET IC process and circuits and the HP Root nonlinear FET model. He is currently responsible for MMIC circuit development, IC packaging, and an HBT IC project.

Dr. Kondoh is a member of the IEEE MTT, ED, and LEOS Societies and the IEICE of Japan.